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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/538,576
Filing Date: June 15, 2005
Appellant(s): VAN HOUDT ET AL.

Robert J. Crawford
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 09/10/09 appealing from the Office action mailed 08/22/08.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4744081	Buckland	05-1988
7035292	Giorgetta et al	04-2006

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-14 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Buckland (U.S. Pat. No. 4744081).

Regarding claim 1, Buckland discloses a frame synchronizing (abstract) device for a binary data transmission system wherein digital data are transmitted as a serial bit stream (fig. 1, ref. 24) organized into frames (col. 1, lines 5-15; see also fig. 3), each frame including a pre-defined frameheader (i.e. “frame word"; col. 1, lines 20-25), comprising: a serial input (fig. 1, ref. 24) parallel output (fig. 1, “m”) shift register (fig. 1, refs. 16 and 18) for receiving said serial bit stream (fig. 1, “SERIAL DATA”) and outputting said frames (fig. 1, “PARALLEL DATA”) in a consecutive order, said shift register (fig. 1, refs. 16 and 18) including a serial input portion (fig. 1, ref. 16) and a parallel output portion (fig. 1, “m”, ref. 18) and having at least m stages (“m-bit words”; col. 2, line 65) as the number of bits in a frame (see discussion below), first clock circuitry (inherent, but not illustrated; generates "SERIAL CLOCK" 25) that generates first clock pulses, separated by a first time period (i.e. “one pulse" period; col. 3, line 31), for clocking the serial input portion (fig. 1, ref. 16) of the shift register; second clock

circuitry (fig. 1, ref. 20) that generates second clock pulses (fig. 1, “CLOCK") for clocking the parallel output portion (fig. 1, ref. 18) of the shift register, the second clock circuitry generating the second clock pulses responsive to the first clock pulses, and controlling circuitry (*inter alia*, fig. 1, refs. 20, 22, 14, and 12) for detecting (fig. 1, ref. 14) whether or not a frameheader or “frame word” (fig. 1, “FRAME WORD”) is present at the output of said parallel output portion and, if not, controlling (fig. 1, ref. 10; "SLIP”) said shift register so that the clocking of the parallel output portion is delayed by at least the first time period (i.e. “one pulse" period; col. 3, line 31, the control circuitry delaying the clocking of the parallel output portion (col. 3, lines 33-39) by preventing one of the first clock pulses from reaching the second clock circuitry (i.e. "to cause the divided to slip by one pulse of the serial clock on the line 26"; col. 3, lines 30-32). Buckland discloses that the serial input / parallel output shift register is the length of m-bits (fig. 1, ref. 16; col. 2, line 65). As broadly as claimed, each of Buckland's 8 bit search positions (see fig. 3) is considered to be a “frame”. Therefore, the shift register has “at least as many stages as the number of bits of a frame” because it contains m bits (m is disclosed as 8 bits; col. 2, line 27) and m bits constitutes the length of a frame. As is conventionally understood, Buckland's 512 x 8 bits is considered a superframe. Finally, as broadly as claimed, Buckland’s SLIP signal (see figure 1) “prevents one of the first clock pulses from reaching the second clock circuitry” because it causes the second clock circuitry (fig. 1, ref. 20) to "slip by", overlook, or not act upon “one pulse of the serial clock”.

Regarding claim 2, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses that said controlling means is adapted so that the

delay of the outputting of a frame is repeated several times until synchronization is reached (col. 2, lines 10-20).

Regarding claim 3, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses that the frames have a fixed length of 8 bits as applied in claim 1 above.

Regarding claim 4, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses that the frames are bytes (i.e. 8 bits each) as applied to claim 1 above.

Regarding claim 5, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses a first clock means (fig. 1, ref. 20) for generating first clock pulses (fig. 1, “CLOCK”) clocking said parallel output portion (fig. 1, ref. 18) of said shift register means (fig. 1, refs. 16 and 18), wherein controlling means are adapted to control (via "SLIP" control; fig. 1) said first clock means so that said first clock pulses are delayed by at least one time period which is needed for shifting a bit in said serial input portion from a stage to a next one (col. 3, lines 20-40).

Regarding claim 6, Buckland discloses the limitations of claim 5 as applied above. Further, Buckland discloses that each frame (including the frame word) includes N or m bits (i.e. “N” = "m"; fig. 1; col. 37-39), a second clock means (not shown) is provided for generating second clock pulses (fig. 1, ref. 25) for clocking said serial input portion of said shift register means, and said first clock means (fig. 1, ref. 20) converts said second clock pulses into said first clock pulses (fig. 1, “CLOCK”) having a time period which is N or m times (i.e. “N” – “m”; fig. 1, ref. 20, (÷ m DIVIDER”) longer than

the time period of said second clock pulses, characterized in that said controlling means is adapted to control said first clock means so that said first clock pulses are delayed by at least one time period of said second clock pulses (col. 3, lines 20-40).

Regarding claim 7, Buckland discloses the limitations of claim 5 as applied above. Further, Buckland discloses that said controlling means is adapted to supply a ("kick-pin") control signal (fig. 1, output of control circuit 10; "SLIP") to said first clock means (fig. 1, ref. 20), and said first clock means is adapted so that its output is modified by said control signal for at least one time period which is needed for shifting a bit in said serial input portion of said shift register means from a stage to a next one (col. 3, lines 20-40).

Regarding claim 8, Buckland discloses the limitations of the claim as applied to claim 1 above.

Regarding claim 9, Buckland discloses the limitations of claim 8 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 2 above.

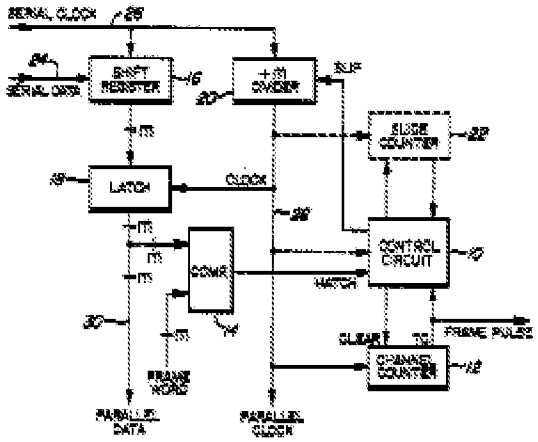
Regarding claim 10, Buckland discloses the limitations of claim 8 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 3 above.

Regarding claim 11, Buckland discloses the limitations of claim 10 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 4 above.

Regarding claim 12, Buckland discloses the limitations of claim 8 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 5 above.

Regarding claim 13, Buckland discloses the limitations of claim 12 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 5 above.

Regarding claim 14, Buckland discloses the limitations of claim 12 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 5 above.



Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Buckland in view of Giorgetta et al (U.S. Pat. No. 7035292; "Giorgetta").

Regarding claim 15, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses that serial data is transported over a single channel (fig. 1, ref. 24) and, at the receiving side, is converted into parallel data (fig. 1, “m”) for further processing. Buckland does not disclose the use of the device in a digital data transmission systems like SONET/SDH or Gigabit Ethernet. However, systems like SONET/SDH or Gigabit Ethernet are well known in the art as suggested by Giorgetta (col. 3, lines 20-30). Further, Giorgetta discloses synchronizing to a frame (col. 7, lines 1-30). In view of the disclosure of Giorgetta, one skilled in the art would have recognized that the exemplary frame synchronization device of Buckland is capable of frame synchronization in SONET and Gigabit Ethernet applications. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the device of Buckland could be applied as a frame synchronization device in a SONET or Gigabit Ethernet application as suggested by Giorgetta because such applications require frame synchronization and are well known in the art.

(10) Response to Argument

The Applicant suggests that the prior art reference Buckland (U.S. Pat. No. 4744081) fails to disclose control circuitry "delaying the clocking of the parallel output portion by preventing one of the first clock pulses from reaching the second clock circuitry."

As applied in the Examiner's final rejection dated August 22, 2008, the claimed first clock pulse is disclosed by Buckland's "SERIAL CLOCK" (fig. 1, ref. 26). The parallel output portion is Buckland's "LATCH" (fig. 1, ref. 18). The parallel output portion is clocked by the "CLOCK" (fig. 1) output from Buckland's clock divider (fig. 1, ref. 20). The clock divider is applied as the claimed second clock circuitry. The second clock circuitry or clock divider is driven by the first clock pulse. Finally, the second clock circuitry takes as input a "SLIP" signal (fig. 1) from Buckland's control circuit (fig. 1, ref. 10) that "prevents" the second clock circuitry from acting upon any received pulses of the first clock.

The Applicant notes that Buckland illustrates a direct connection of the first clock pulse (i.e. "SERIAL CLOCK") to the second clock circuitry (fig. 1, ref. 20) and argues that, because of the direct connection, Buckland can not cover the claimed "preventing one of the first clock pulses from reaching the second clock circuitry." However, Buckland discloses in column 2, lines 60-65:

"The serial clock signal is also supplied to the divider 20 which, in the absence of a signal SLIP supplied from the control circuit 10, frequency divides the clock signal by a factor M to produce a clock signal on a line 28, under the control of which m-bit words from the shift register 16 are latched in the latch 18 (emphasis added)." In column 3, lines 28-33, Buckland also discloses "in this case the slide counter 22 is reset and the control circuit 10 supplies the signal SLIP to the divider 20 to cause the divider to slip by one pulse of the serial clock on the line 26. i.e. to divide by m-1 or m+1 for one division cycle.

It is certain that Buckland's second clock circuitry 20 "frequency divides" the first clock pulses. However, Buckland clearly discloses that the second clock circuitry 20 only performs such dividing in the absence of a signal SLIP supplied from the control circuit 10. That is, the first clock pulses are **"prevented"** from being divided or are **"prevented"** from reaching the divider of the second clock circuitry in the condition that the SLIP signal is present because such pulses are only divided if the SLIP signal is not present.

The Applicant, in essence, argues that the lack of a specific "gating control circuit" between the first clock pulses and the second clock circuitry in Buckland's figure 1 is determinative on the point. However, although Buckland does not illustrate such a specific "gating control circuit", Buckland does disclose control circuitry (fig. 1, ref. 10) which outputs a SLIP signal which is applied in the second clock circuitry (fig. 1, ref. 20) as a "gate" to the operation of the circuitry's dividing operation.

With respect to the Applicant's argument that no motivation is shown to combine the prior art references Buckland and Giorgetta et al (U.S. Pat. No. 7035292; "Giorgetta"), the argument is not persuasive. Buckland's frame finding circuitry could be advantageously utilized in an optical receiver and the combination of the two references would produce only routine and predictable results.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Temesghen Ghebretinsae/

Primary Examiner, Art Unit 2611

1/3/2010.

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